IN THE CLAIMS

1. (Withdrawn) A data processing control apparatus that alternatively makes one among a plurality of service executers each designed to execute predetermined service execute service, comprising:

a controller for performing control so that whichever of the service executers requested to execute service is given a highest order of priority executes service;

a priority updater for updating orders of priority given to the individual service executers in such a way that, every time a given service executer has continuously executed an amount of service that a single service executer is permitted to continuously execute, the given service executer is given a lowest order of priority; and

a memory for storing, for each of the service executers, data indicating amount of service that a single service executer is permitted to continuously execute.

2. (Currently Amended) A DMA controller comprising:

a ~~setting~~ first register for permitting a CPU to make ~~settings for~~ DMA transfer therein, the first register being capable of storing data;

~~an operation register for permitting data stored in the setting register to be written thereto, or~~ an operation counter for performing counting operation by use of the data stored in the first register;

an operation controller for performing control so that, when DMA transfer is started, ~~the~~ an occurrence of data storage ~~stored~~ in the ~~setting~~ first register is ~~written to the operation register or~~ counted by the operation counter; and

a transfer executer for executing DMA transfer based on ~~the data stored in the operation register or~~ the operation counter.

3. (Original) A DMA controller comprising:

an operation register for storing transfer conditions under which DMA transfer is currently being executed;

a setting register for storing transfer conditions under which DMA transfer is to be executed next time;

a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register;

a selector for alternatively selecting one of the setting register and the setting execution register;

a selection controller for performing control so that the register selected by the selector is switched alternately between the setting register and the setting execution register every time DMA transfer ends;

an operation register controller for performing control so that, when DMA transfer is started, data stored in the register selected by the selector is written to the operation register; and

a transfer executer for executing DMA transfer based on the data stored in the operation register.

4. (Withdrawn) A data processing apparatus comprising a CPU for

executing a program and a memory for storing data or for storing data and the program wherein the data can be read out from the memory through a data processing control apparatus, the data processing control apparatus alternatively making one among a plurality of service executers each designed to execute predetermined service execute service, the data processing control apparatus comprising:

a controller for performing control so that whichever of the service executers requested to execute service is given a highest order of priority executes service;

a priority updater for updating orders of priority given to the individual service executers in such a way that, every time a given service executer has continuously executed an amount of service that a single service executer is permitted to continuously execute, the given service executer is given a lowest order of priority; and

a memory for storing, for each of the service executers, data indicating amount of service that a single service executer is permitted to continuously execute.

5. (Currently Amended) A data processing apparatus comprising a CPU for executing a program and a memory for storing data or for storing data and the program wherein the data can be read out from the memory through a DMA controller,

the DMA controller comprising:

a ~~setting~~ first register for permitting a CPU to make ~~settings for~~ DMA transfer therein, the first register being capable of storing data;

~~an operation register for permitting data stored in the setting register to be written thereto, or~~ an operation counter for performing counting operation by use of the data stored in the first register;

an operation controller for performing control so that, when DMA transfer is started, ~~the~~ an occurrence of data storage ~~stored~~ in the ~~setting~~ first register is ~~written to the operation register or~~ counted by the operation counter; and

a transfer executer for executing DMA transfer based on ~~the data stored in the operation register or~~ the operation counter.

6. (Original) A data processing apparatus comprising a CPU for executing a program and a memory for storing data or for storing data and the program wherein the data can be read out from the memory through a DMA controller, the DMA controller comprising:

an operation register for storing transfer conditions under which DMA transfer is currently being executed;

a setting register for storing transfer conditions under which DMA transfer is to be executed next time;

a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register;

a selector for alternatively selecting one of the setting register and the setting execution register;

a selection controller for performing control so that the register selected by the selector is switched alternately between the setting register and the setting execution register every time DMA transfer ends; an operation register controller for performing

control so that, when DMA transfer is started, data stored in the register selected by the selector is written to the operation register; and

a transfer executer for executing DMA transfer based on the data stored in the operation register.

7. (New) A DMA controller according to claim 2,

wherein the first register is adapted to make settings for DMA transfer, and

the DMA controller further comprises a second register for permitting data stored in the first register to be written thereto,

wherein the operation controller is adapted to perform control so that, when DMA transfer is started, the data stored in the first register is written to the second register, and

wherein the transfer executer is adapted to execute the DMA transfer based on the data stored in the second register.

8. (New) A DMA controller according to claim 2, further comprising:

a third register for permitting the CPU to make DMA transfer therein, the third register being capable of storing data;

a second operation counter for performing counting operation by use of the data stored in the third register; and

a second operation controller for performing control so that, when DMA transfer is started, an occurrence of data storage in the third register is counted by the second operation counter,

wherein the transfer executer is adapted to execute DMA transfer based on the first and second operation counters.

9. (New) A DMA controller according to claim 8, further comprising:

a second register for permitting data stored in the first register to be written thereto; and

a fourth register for permitting data stored in the third register to be written thereto,

wherein the first mentioned operation controller is adapted to perform control so that, when DMA transfer is started, the data stored in the first register is written to the second register, and the second operation controller is adapted to perform control so that, when DMA transfer is started, the data stored in the third register is written to the fourth register, and

wherein the transfer executer is adapted to execute the DMA transfer based on the data stored in one of the second and fourth registers.